IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of programming a FLASH memory device comprising:

issuing a blank check command to a command register within the FLASH memory device, wherein the blank check command specifies a specified block to blank check;

~~reading a status bit in a status register within the FLASH memory device to verify that at least a portion of the FLASH memory device is blank; and~~

checking a signal level on a conductor coupled to the FLASH memory device to verify that the specified block is blank; and

programming memory locations within the ~~portion~~ specified block of the FLASH memory device ~~verified as blank~~.

2. (Currently Amended) The method of claim 1 further comprising checking a busy bit in the FLASH memory device adapted to signify that the ~~status bit~~ signal level on the conductor is valid.

3. (Original) The method of claim 1 wherein issuing a blank check command comprises:

issuing a blank check setup command; and

issuing a blank check confirm command.

4. (Canceled).

5. (Currently Amended) The method of claim [[4]] 1 further comprising repeating the ~~method~~ issuing, checking, and programming for more than one block in the memory device.

6. (Currently Amended) The method of claim [[4]] 1 further comprising repeating the ~~method~~ issuing, checking, and programming for each block in the memory device.

7. (Currently Amended) A method of blank checking and programming a FLASH memory device comprising:

receiving a blank check command from a device external to the FLASH memory device, wherein the blank check command specifies a specified block to blank check;

in response to the blank check command received from a device external to the FLASH memory device, reading a plurality of memory locations in ~~at least one~~ the specified block of the FLASH memory device;

~~writing to a bit in a status register to indicate whether the at least one block is blank, wherein the status register is accessible by the device external to the FLASH memory device; and~~

asserting a signal on a conductor coupled to the device external to the FLASH memory device to signify that the specified block is blank; and

receiving data to be programmed in the ~~at least one~~ specified block.

8. (Original) The method of claim 7 wherein receiving a blank check command comprises:

receiving a blank check setup command; and

receiving a blank check confirm command.

9. (Currently Amended) The method of claim 7 wherein reading a plurality of memory locations comprises reading each memory location in the ~~at least one~~ specified block.

10. (Currently Amended) The method of claim 7 further comprising:

setting a busy bit adapted to signify the FLASH memory device is busy; and

clearing the busy bit after ~~writing to the bit in the status register~~ asserting the signal on the conductor to signify that the specified block is blank.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) A memory device comprising:

a FLASH memory core;

a control block adapted to blank check ~~at least a portion~~ a specified block of the FLASH memory core; and

an external interface to allow communication between the control block and a device external to the memory device, the external interface including a command register to receive a blank check command that specifies the specified block, wherein the control block is capable of blank checking the ~~at least a portion~~ specified block of the FLASH memory core during a programming operation when the memory device is in use in a system, and wherein the control block is further capable of asserting a signal on a conductor external to the memory device to signify that the specified block is blank.

14. (Currently Amended) The memory device of claim 13 wherein the external interface comprises a status register adapted to signify that the ~~at least a portion of the FLASH memory core is blank~~ memory device is busy.

15. (Original) The memory device of claim 13 wherein the control block comprises a state machine.

16. (Original) The memory device of claim 13 wherein the control block comprises a microcontroller.

17. (Canceled)

18. (Currently Amended) The memory device of claim ~~17~~ 13 wherein the external interface further includes a status register.

19. (Currently Amended) An apparatus including a medium adapted to hold machine-accessible instructions that when accessed result in a machine performing:

issuing a blank check command to a command register within a FLASH memory device, wherein the blank check command specifies a specified block to blank check;

~~reading a status bit in a status register within the FLASH memory device to verify that at least a portion of the FLASH memory device is blank; and~~

checking a signal level on a conductor coupled to the FLASH memory device to verify that the specified block is blank; and

programming memory locations within the ~~portion~~ specified block of the FLASH memory device verified as blank.

20. (Currently Amended) The apparatus of claim 19 wherein the instructions, when accessed, further result in the machine performing:

checking a busy bit prior to ~~reading the status bit~~ checking the signal level on the conductor coupled to the FLASH memory.

21. (Original) The apparatus of claim 19 wherein issuing a blank check command comprises:

issuing a blank check setup command; and

issuing a blank check confirm command.

22. (Currently Amended) The apparatus of claim 19 wherein the instructions, when accessed, further result in the machine performing:

issuing blank check commands and ~~reading the status bit~~ checking the signal level on the conductor for more than one block in the memory device.

23. (Currently Amended) An electronic system comprising:

a direct conversion receiver;

a processor coupled to the direct conversion receiver; and

a memory device coupled to the processor, the memory device including a FLASH memory core, a control block adapted to blank check ~~at least a portion~~ a specified block of the FLASH memory core, and an external interface to allow communication between the control block and the processor, the external interface including a command register to receive a blank

check command that specifies the specified block, wherein the control block is capable of blank checking the ~~at least a portion~~ specified block of the FLASH memory core during a programming operation by the processor, and wherein the control block is further capable of asserting a signal on a conductor external to the memory device to signify that the specified block is blank.

24. (Original) The electronic system of claim 23 wherein the control block comprises a microcontroller.

25. (Canceled)

26. (Currently Amended) An electronic system comprising:

a direct conversion receiver;

a FLASH memory device;

a processor coupled to the direct conversion receiver and the FLASH memory device; and

an article having a machine accessible medium holding instruction that when accessed result in the processor issuing a blank check command to a command register within the FLASH memory device wherein the blank check command specifies a specified block to blank check, ~~reading a status bit in a status register within the FLASH memory device to verify that at least a portion of the FLASH memory device is blank~~ checking a signal level on a conductor coupled to the FLASH memory device to verify that the specified block is blank, and programming memory locations within the ~~portion~~ specified block of the FLASH memory device verified as blank.

27. (Original) The electronic system of claim 26 wherein issuing a blank check command comprises:

issuing a blank check setup command; and

issuing a blank check confirm command.

28. (Currently Amended) The electronic system of claim 26 wherein the instructions, when accessed, further result in the machine performing:

issuing blank check commands and ~~reading the status bit~~ checking the signal level on the conductor for more than one block in the FLASH memory device.